**Question 3**

There are no special use cases or requirements in this program.

This is the same as question 2, but with 2 crucial differences. The first is that the output is clocked – in other words, it only changes on the rising edge of the clock. The second is that there is a reset signal enabled; it is a synchronous reset, so it only triggers on the rising edge of the clock.

The test bench consists of 4 parts:

1) NUM1 = 8, NUM2 = 4, RESET = 0 -> Result is based on SELECT at the beginning of the clock signal

2) NUM1 = 9, NUM2 = 7, RESET = 0

3) NUM1 = 15, NUM2 = 10, RESET = 0

4) RESET = 1 -> Result should be 0 on Clock Cycle after RESET goes high until CLK cycle after RESET goes low

